Defence Science Journal, Vol 48, No 4, October 1998, pp. 423-431

Silicon Membranes for Smart Silicon Sensors

S. Kal, S. Das and S. K. Lahiri
Indian Institute of Technology, Kharagpur - 721 302

ABSTRACT

The development of smart *Si* sensors which combine active circuitry and sensor on the same chip, has drawn attention in terms of miniaturisation and cost-effectiveness of microsensors. Interest in micromachining of *Si* to fabricate membranes derives from the need for inexpensive and more versatile sensors. This paper reports the results on fabrication of *Si* membranes by anisotropic etching of *Si* in EDP solution. Good quality membranes of 10 μm thickness were fabricated. Infrared detector based on thermopile structure was realised on 50 μm thick *Si* membrane using polysilicon and *Al* junctions. Thermo-emf generated at 150 °C is nearly 8 mV.

1. INTRODUCTION

Micromachined sensors and actuators operating in the fascinating interface between electronics and physics is an attractive and promising area of research in the frame work of integrated circuit technology with its possibilities and novelties. Silicon has shown itself to be the best material for this technology because it shows many pronounced physical effects which can be used for sensing purposes[1,2]. Silicon micromachining is of great importance for the development of inexpensive, batch fabricated, high performance sensors, which can easily be interfaced with microprocessors. Batch-fabricated *Si* integrated sensors are now replacing expensive discrete sensors. Membranes are integral parts of many *Si* integrated sensors, viz., temperature or pressure sensors[3,4]. This paper reports some results of the micromachining of *Si* and fabrication of a high speed thermopile IR sensor on *Si* membrane.

2. MICROMACHINING OF SILICON & FABRICATION OF SILICON MEMBRANES

The following properties of *Si* have made micromachining feasible:

(a) Silicon can be readily oxidised by exposing it to steam or dry O_2. It allows *Si* wafer to be masked selectively during chemical etching.

(b) Single crystal *Si* is brittle and can be cleaved like diamond, but it is harder than most metals. It is resistant to mechanical stresses, and the elastic limit of *Si* is greater than that of steel.

(c) A single crystal *Si* can withstand repeated cycles of compressive and tensile stresses.

(d) The crystal orientation of single crystal *Si* wafer decides the rate of chemical etching in certain etching solutions, which is important in creating various structures.

The selective etching of *Si* can be carried out by using both isotropic and anisotropic etchants. Isotropic etchant under-etch large area in lateral

Received 12 August 1997, revised 18 March 1998

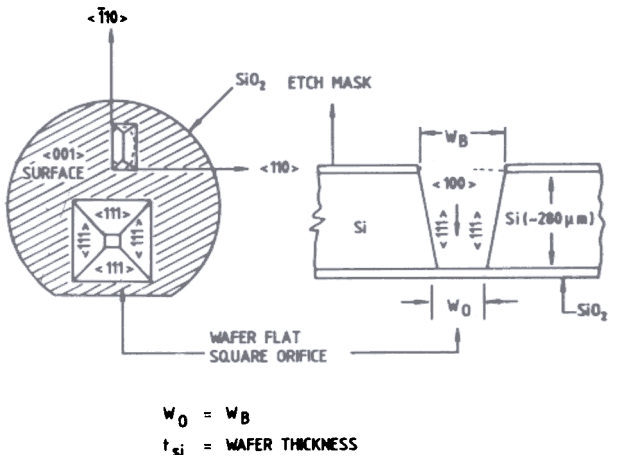

Figure 1. Schematic of anisotropic etch-profile on silicon wafer

directions than the area defined by mask opening. On the other hand, anisotropic etchant, which is also known as orientation-dependent or crystallographic etchant, etches the *Si* surface at different rates in different directions in the crystal lattice. They can form well-defined shapes with sharp edges and corners[5]. The two most widely used anisotropic etchant are EDP and *KOH*. EDP etchant is a mixture of ethylenediamine (EN), pyrocatechol and H_2O [6]. Potassium hydroxide etchant exhibits a much higher (110) to (111) etch rate ratios than EDP. A disadvantage of *KOH* is that SiO_2 is etched at a rate which preclude use of SiO_2 as mask in many applications. In structures requiring long etchant times, Si_3N_4 is the preferred masking material for *KOH*. The etch-stop technique used for *KOH* etchant poses another difficulty. The electrochemically-controlled etch-stop technique used in this type of etchant, requires a complex setup with *Pt* electrodes and a vacuum holder for the wafer.

EDP etchant has main advantage that it is highly selective over materials like SiO_2, Si_3N_4, *Cr* and *Au*. Also etch-stop technique used in case of EDP is very simple. These two reasons are sufficient to make use of EDP a popular choice. The anisotropic etch rate of EDP solution depends on the temperature, composition of the etchant and the density of atomic bonds on an exposed *Si* plane. The exposed <111> planes are etched slowly, <110> planes are usually etched rapidly and <100> planes are etched at an intermediate rate. Etched holes may have only <111> and <100> facets. The *Si* wafers are mostly used for anisotropic etching, such as <100> wafers and <110> wafers. The orientation, size and shape of the oxide opening on the wafer surface also play a part in determining the type of hole formed. For examples, if a square hole is opened in an oxide layer on a <100> wafer, treatment with anisotropic etchant can create an upside down pyramid pit. Four sets of <111> planes intersect the surface of a <100> wafer along the two perpendicular <110> directions that lie in the surface plane. During anisotropic etching, the exposed <100> surface plane is etched downwards at a constant rate, giving the pit a flat bottom at the end of the etch process. At the edges of hole, four inward slanting <111> planes form the walls of the pit. As etching continues, more of the <111> planes is exposed and the area of the flat bottom shrinks. Eventually, the <111> planes meet at a point and the flat bottom is gone. The etching then stops because no readily attacked planes are exposed. Figure 1 shows the schematic of etching profile on *Si* wafer. The size of the oxide pattern determines not only the area of the pit on the wafer surface but also the depth of the pit. The longer the square oxide opening, the deeper the point at which the <111> side walls of the pit intersect. If the oxide opening is large enough, the <111> planes do not intersect within the wafer. The etched pit, therefore, extends all the way through the wafer, creating a small square opening on the bottom surface. It is, therefore, evident that shape and size of the oxide opening can decide the structure of etched pit. In this way V-groove, trench, pyramid, membrane, cantilever, etc. can be easily formed by micromachining of *Si*.

A simpler way to achieve a thin membrane would have been to etch a wafer for a period just short of what it would take to etch through it. But it is difficult to make membrane of uniform thickness by this method, because the thickness of the membrane is determined by that of the wafer, and the wafer thickness varies typically by 10 μm or more both across a single wafer and from one wafer

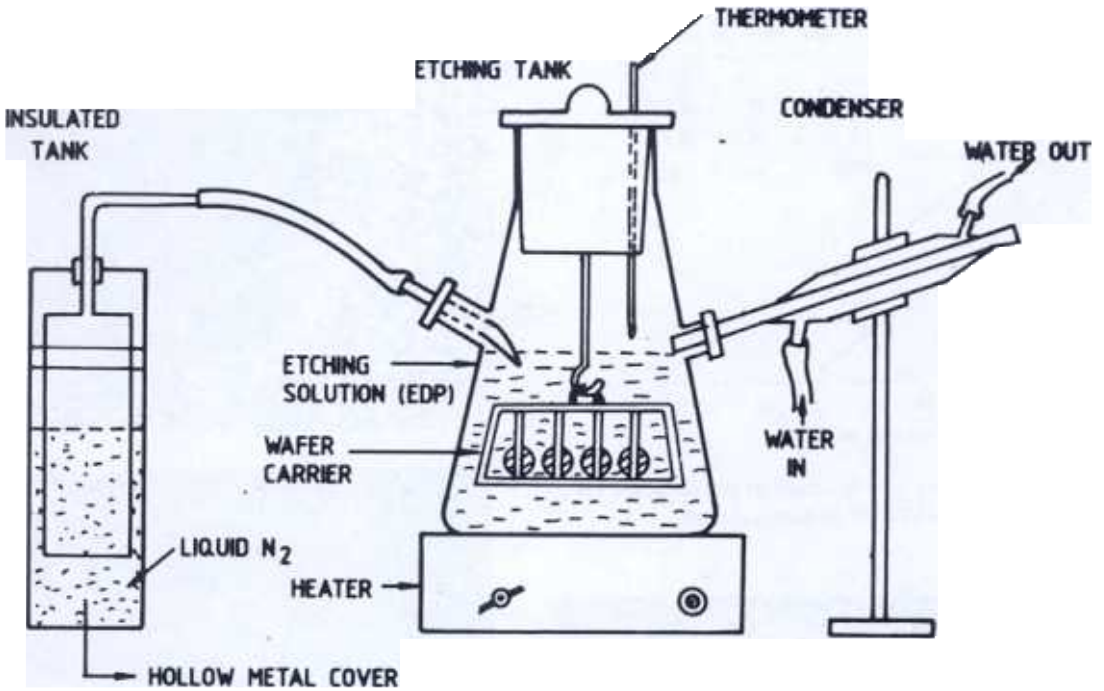

Figure 2. Experimental setup for silicc ı membrane etching using EDP solution

to another. Membranes of more precisely defined thickness and shape can be created by a technique that exploits another property of anisotropic etchant. The rate at which the solution etches a wafer depends also on the extent to which the *Si* is doped with impurity atoms[7]. For examples, the anisotropic etchant like EDP etches heavily boron-doped *Si* at a much slower rate than lightly boron-doped *Si*. Therefore to control the membrane thickness, a precisely defined junction depth of boron could be created by the standard process of pre-deposition and drive-in diffusions. The thickness of the heavily boron-doped layer will be the thickness of the membrane.

The first step of reaction in the EDP solution is the ionisation step, where EN combines with H_2O to give free $(OH)^-$ radical. Therefore, it is evident that H_2O is the part of the reaction and is not a diluting agent. Pyrocatechol is a complexing agent which forms complexes with the reaction products on the *Si* surface. The complex pyrocatecholate is soluble in EN. Oxidation-reduction reaction follows after ionisation reaction step.

3. MEMBRANE ETCHING PROCESS

The first step in creating a membrane is to grow a thick and defect-free pure SiO_2 by thermal oxidation. The thermal oxide layer is used to protect the backside of *Si* wafer during boron diffusion in the front side for creating a *p*-stop layer. The boron concentration required to create a *p*-stop layer should be 10^{19}-10^{20} atoms/cc. The thickness of the membrane is decided by boron diffusion depth. Boron was diffused in *Si* from a solid source BN-1100. The pre-deposition diffusion was done at 1100 °C for 30 min. followed by drive-in diffusion at 1175 °C for 10-150-20 min. in dry-wet-dry O_2 atmosphere. The diffusion parameters were decided from the process simulation results using SUPREM to have concentration nearly 10^{20} atoms/cc. After etch-stop boron diffusion, windows for membrane were opened by photolithography. During *Si* etch, SiO_2 acts as mask whose etch rate in EDP solution is about 20 nm/hr compared to 30-50 μm/hr for *Si*. The quality of mask oxide plays a very important role in *Si* etching process. The purity of O_2 used in oxidation, porosity in SiO_2, oxide thickness and

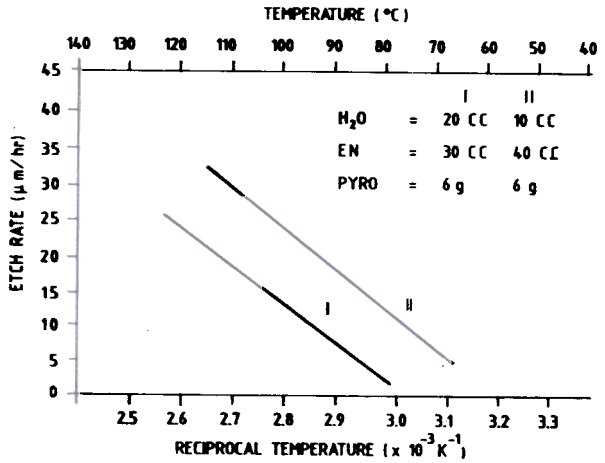

Figure 3. Etch rate of silicon as a function of temperature for two compositions of EDP etching solution.

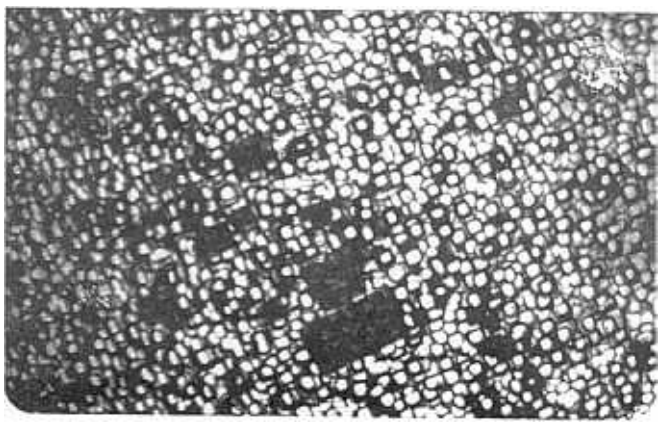

Figure 4. Photomicrograph of etch pits formed on SiO_2 surface when etching done at a higher temperature.

temperature of EDP solution contribute to the successful etching of *Si*-membranes[4,8].

The EDP etching solution was prepared using 49.6 mole per cent H_2O (112 cc), 46.4 mole per cent EN (387 cc) and 4 mole per cent pyrocatechol (55 g). The mixture was stirred well in a beaker to dissolve pyrocatechol and then poured into a special etching tank which had an inlet for N_2 gas flow and an outlet for condensation. The membrane etching arrangement is shown in Fig. 2. Ethylenediamine is highly toxic and corrosive chemical, and readily gets oxidised. So, a stream of N_2 was bubbled through the etching solution to prevent oxidation of the amine and to provide agitation of the sample. A H_2O cooling system was provided to avoid the evaporation of volatile substrates at high

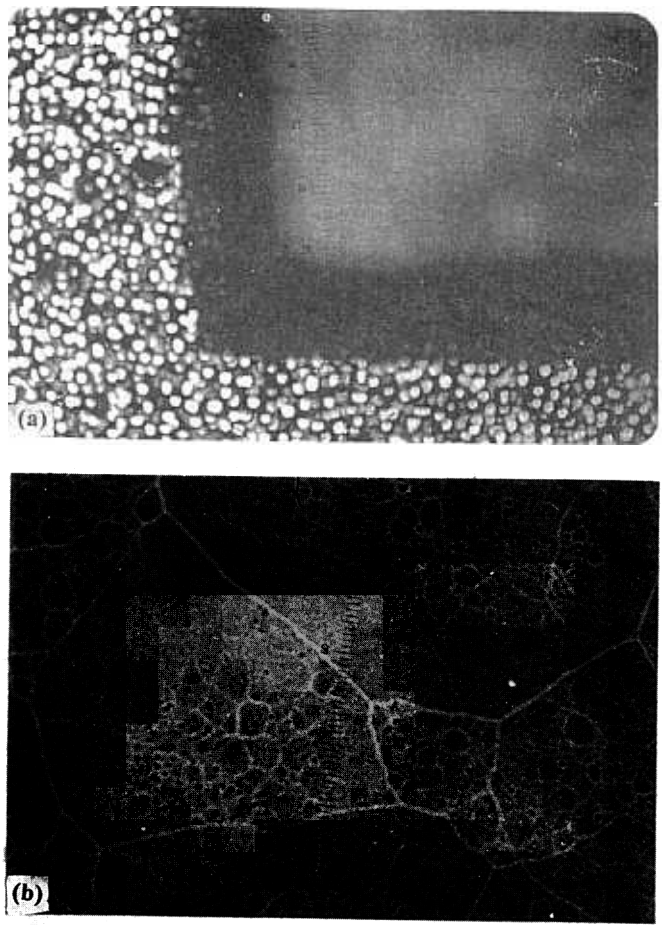

Figure 5. Photomicrograph of silicon membrane fabricated by anisotropic EDP etching.

temperature. The temperature of the EDP etchant was maintained at 100 °C during etching and the etch rate was 35 μm/hr. The temperature dependence of etch rate of *Si* in EDP solution for two different composition is shown in Fig. 3. The etch rate was determined by measuring the step profile using Taylor-Hobson laser profiler. The results indicate that the etch rate is faster, and the selectivity of *Si* etching decreases when the etching is carried out at a temperature more than 125 °C. Pin holes and etch pits were found on oxide surface when etching was done at a higher temperature. Photomicrograph of Fig. 4. shows such types of square etch pit. Black squared regions in Fig. 4 are the etch pits. The temperature range of 100-125 °C was found suitable for the membrane etching using EDP, especially when the substrate is required to be processed further. After the etching was completed, the wafer was thoroughly cleaned in DI water and

dried under laminar flow. The photomicrograph of the *Si* membrane fabricated by EDP etching is shown in Figs 5(a)-(b). In Fig. 5(a), illuminated region is the membrane formed after *Si* etching, whereas black region is the substrate. Illuminated and focussed membrane is shown in Fig.5 (b). Substrate surface is out of focus and is seen black here.

4. DESIGN & FABRICATION OF INFRARED DETECTOR

A large spectrum of emitted radiation from a hot body lies in the IR region. The relation between the body temperature and frequency spectrum of emitted radiation can be used to find the temperature of the body. Two fundamental IR detectors available today are thermal detectors and photon detectors. The two-step transduction process of thermal detector is considerably slower than the single-step process associated with photon devices. However, in applications where high speed is not of primary importance, the thermal detectors have a number of advantages, including a broad spectral response, low cost, ease of operation and insensitivity to ambient temperature. Among thermal detectors, two of the most common detectors are thermopile and pyroelectric devices. Thermopile detectors require no bias voltage and are used over a wider temperature range and easily interfaced with monolithic circuitry. When a number of thermocouples are joined in series to amplify the output voltage, they are called thermopile detectors. The advantage of thermocouple is that it comes to thermal equilibrium quite rapidly in the system because of its small mass[9,10]. The thermopile detectors make use of Seebeck effect which arises from the fact that the density of charge carriers (electron in metal) differs from one conductor to another and depends upon the temperature. The basic *Si* thermopile IR detector structure is shown in Fig. 6. It consists of a series of thermocouples whose hot junctions are supported by a thin *Si* membrane (window) and whose cold junctions are on the thick chip rim. Since the boron-doped p^+ membrane is a good electrical conductor, the couples must be insulated

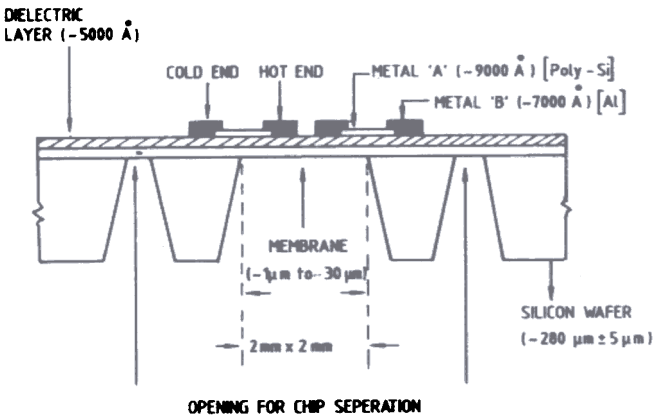

Figure 6. Basic silicon thermopile IR detector structure

from the membrane. Chemicalvapour deposition (CVD) grown SiO_2 is used as a insulated layer. The metal A and B constitute the thermocouple. In our lstudy, doped-poly *Si* and *Al* are used as metal A and metal B, respectively. The membrane area is generally coated with a thin layer of an absorbing material, such as bismuth black, so that energy incident on the chip is absorbed efficiently over a broad spectral range from visible to far infrared. The thermal conductivity of the *Si* membrane is a relatively strong function of doping concentration. It is evident that the *Si* membrane has the lowest thermal resistance and cannot be easily loaded with any other material. For a temperature difference, ΔT between the hot and cold junctions, a voltage will be developed across the thermopile which is equal to

$$V = N \alpha_s \Delta T \tag{1}$$

where α_s is the Seebeck coefficient of the two materials and N is the total number of couples. In addition to the d.c. response, it is useful to compute the transient response of the device. The time constant of a thermopile radiation detector is defined as

$$\tau = R_{th} \cdot C_{th} \tag{2}$$

where C_{th} is the thermal capacitance of the window and R_{th} is the thermal resistance between the appropriate tap point in the resistor string and the

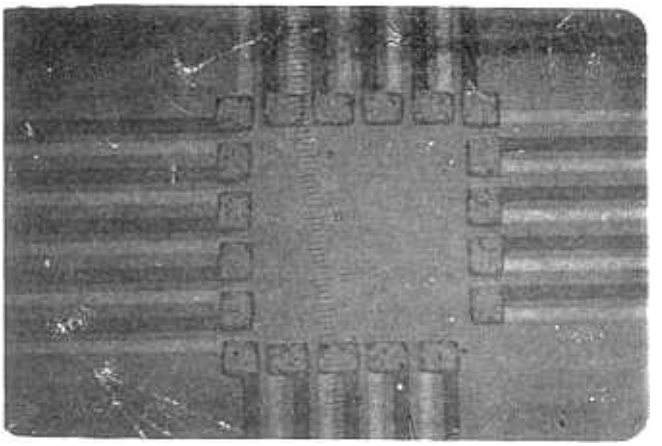

Figure 7. Photomicrograph of a fabricated thermopile IR detector.

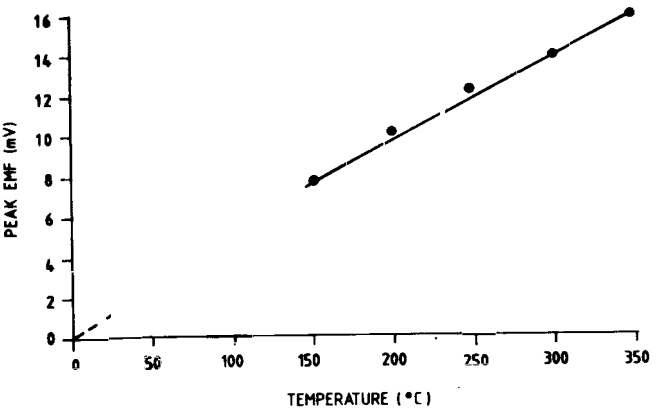

Figure 8. Plot of peak emf *vs* hot-probe temperature of thermopile structure.

rim. A figure of merit for a thermocouple material is defined as

$$Z = (\alpha^2 \sigma)/k \quad (3)$$

where α is thermoelectric power, σ is electrical conductivity and k is thermal conductivity. The materials for thermopile are selected such that they can be deposited and patterned easily on *Si* and SiO_2, have good adhesion on SiO_2, have higher figure of merit and low time constant. Polysilicon and *Al* are chosen for our work on microsensor because (i) they are compatible to each other as far as adhesion and thermo-emf are concerned, (ii) they are easily deposited and patterned, (iii) they produce thermo-emf in the millivolt range, and (iv) they have moderate responsivity and speed.

Initially p^+ etch-stop layer is fabricated by diffusion of boron from the polished front side of the wafer. The temperature and time for the pre-deposition (source: BN-1100) and drive-in diffusion are 1100 °C (30 min) and 1175 °C (150 min), respectively. The diffusion sheet resistance was found to be 2-3 Ω/□. During drive-in diffusion in O_2, insulating SiO_2 layer is grown. Polysilicon and *Al* films were then deposited and patterned sequentially to fabricate the detector structure. Polysilicon film was deposited by ion beam sputtering technique[11]. Oxidised *Si* wafers were loaded into the dual ion beam deposition system and the chamber was evacuated to 10^{-6} Torr. The neutralised *Ar* ion beam bombards on the *Si* target and the sputtered material is deposited on the substrate. The energy and current density of the *Ar* ion beam were typically 1000 eV and 7 mA/cm^2, respectively. The temperature of the substrate was kept at 150 °C during deposition and the deposition rate was 100-120 A/min. The as-deposited polysilicon film was lithographically patterned and annealed at 1000 °C for 30 min in N_2/10 per cent H_2 ambient. Aluminium film was deposited on the patterned polysilicon film and subsequently patterned to get the detector structure. The membranes were then formed by anisotropic EDP etching of *Si* from the backside of the substrate to support the hot junction of the thermocouple. The thermopile is protected from EDP by covering the pattern with special wax which has high melting point (>100 °C). The membrane etching process is discussed in Section II.

The diaphragm is realised by etching through the backside of the wafer after the patterns are formed on the front side. The window regions at backside are aligned with reference to the front side pattern by mask alignment using IR source and video display of the pattern using CCD camera. A special mask alignment test zig was made for this purpose. After membrane etching, wax was removed and the wafers were cleaned thoroughly. The photomicrograph of a fabricated thermopile IR detector is shown in Fig. 7. The number of thermocouple elements connected in series were 19

and the total resistance of the thermopile structure was measured as 134 kΩ. The thickness of polysilicon and *Al* lines were measured by Taylor-Hobson surface profiler and the values were 0.96 μm, and 0.77 μm respectively[4].

A preliminary testing of the thermopile fabricated on *Si* wafer has been carried out to measure the thermo-emf generated by the device. The wafer containing the sensors was placed on the chuck of a probing station and the bondpods of the thermopile were probed. The probes were connected to the input of a sensitive d.c. microvoltmeter. A pointed hot metal probe attached with the hot tip of a soldering iron was brought close to the hot junction of the thermopile and touched with the device surface. Instantaneous change of the thermopile output voltage was recorded in the d.c. microvoltmeter at regular intervals of time. The output voltage first increased rapidly, reached a maximum value and then decreased slowly because of falling temperature difference between the junctions due to the gradual conduction of heat from hot to cold junction. The observations were repeated for different hot-probe temperatures. The temperature of the hot-probe was found by attaching a chromel-alumel thermocouple at the hot region of the membrane. The method of testing was not much accurate and the temperature measurement accuracy was within 5-10 per cent. The plot of peak emf with hot-probe temperature is shown in Fig. 8. The value of thermopile voltage was about 15 μV/ °C above room temperature. The heat loss of hot-probe due to radiation into atmosphere and absorption by test surface, etc. were not taken into account. An accurate measurement setup for testing the thermopile is being developed for transient measurements and accurate measurement of thermo-emf.

5. CONCLUSION

Silicon micromachining and membrane formation techniques described are useful for realising a variety of microelectromechanical sensors and systems (MEMS) for wide ranging applications. The sensitive thermal sensor realised using a series of thermocouples on the *Si* membrane is used in rapid thermal processors in various industries. Membranes are commonly used in pressure sensors.

REFERENCES

1. Peterson, K.E. Silicon as mechanical material. *Proc. IEEE*, 1982, **70**, 420-57.
2. Mo, J. *et al.* Micromachining for improvement of integrated ultrasonic transducer. *IEEE Trans. Electron Devices*, 1990, **37**, 134.
3. Nieveld, G.D. Thermopile fabricated using silicon planar technology. *Sens. & Actuators*, 1983, **3**, 179-83.
4. Chatterjee, G. Development of silicon microsensor for infrared detection. IIT, Kharagpur, 1991. MTech Dissertation (Unpublished).
5. Bassous, E.; Baron, E.F. The fabrication of high precision nozzles by the anisotropic etching of <100> silicon. *J. Electrochem. Soc.*, 1978, **125**(8), 1321-27.
6. Finne, R.M.; Klein, D.A. A water-amine -complexing agent system for etching silicon. *J. Electrochem. Soc.*, 1967, **114** (9) , 965.
7. Bohg, A. Ethylene diamine-pyrocatechol-water mixture shows etching anomaly in boron-doped silicon. *J. Electrochem. Soc.*, 1971, **118**(2), 401-02.
8. Lalchandani, D. Development of smart silicon sensors based on integrated silicon thermopile. IIT, Kharagpur, 1992. MTech Dissertation (Unpublished).
9. Van Herwarreden, A.W. Thermal vacuum sensors based on thermopile. The. Netherlands, 1987. PhD Thesis (Unpublished).
10. Lahiji, G.R.; Wise, K.D., A batch fabricated silicon thermopile infrared detector. *IEEE Trans. Electron Devices*, 1982, **29**(1), 14-22.

    Das, S.; Chaudhuri, A.K.; Lahiri, S.K. Microstructural and electrical characterisation of ion beam sputtered polysilicon films for microelectronic applications. *Thin Solid Films*, 1993, **235**, 215-21.

Contributors

Dr S Kal received his PhD in Electronics & Electrical Communication Engineering from the Indian Institute of Technology (IIT), Kharagpur, in 1983. He visited Ruhr University, Bochum, West Germany, as a DAAD fellow during the period 1984-85 and worked on technology for isoplanar oxide isolated integrated injection logic. He joined IIT, Kharagpur in 1986 and presently, he is Associate Professor in the Department of Electronics & ECE. He visited the University of Erlangen-Nurnberg, Germany, under DAAD re-invitation programme and worked on shallow junction devices for submicron VLSI during May-July 1993. He was awarded International Exchange Fellowship-1997 by INSA, New Delhi and visited Germany for five months. He has published more than 60 research papers in national and international journals. He played a key role in setting up the Microelectronics Centre at IIT for carrying out experimental research in silicon devices and ICs. He has conducted many students' projects and PhD programmes in bipolar devices and ICs. His current research activities include ASICs, metallisation problems in submicron VLSI, special semiconductor films, microsensors and MEMS. He is working in close collaboration with DRDO, ISRO and industries like BEL, Bangalore. He is a member of the Institution of Engineers (India) and IEEE (USA).

Dr S Das received his MSc in Physics from the IIT, Kharagpur, in 1988. He joined at the Microelectronics Centre, Dept. of Electronics and ECE, IIT Kharagpur, in 1989 as a CSIR Research Fellow. He received his PhD in 1996 on large bias conduction in polysilicon, high current pulse trimming of polyresistors and transient studies of polysilicon fuses. Presently, he is working as Scientific Officer in Microelectronics Centre of E & ECE Department. He has been involved in experimental research on ion beam processing for VLSI like dual ion beam deposition of oxynitride films of controllable composition, chemically assisted ion beam etching and polysilicon film deposition and characterisation. He is also involved in the fabrication and characterisation of silicon bipolar devices and integrated circuits, development of micromachining technology and microsensors.

Dr SK Lahiri received his BSc (Physics) from the Presidency College, Calcutta, in 1963, MTech and PhD both from the Institute of Radio Physics & Electronics, Calcutta University in the years 1966 and 1971, respectively. He joined IIT, Kharagpur, in 1971 in the Department of Electronics & Elec. Comm. Engg. He has been working as Professor since 1985. He started his research career in solidstate electronics and SAW devices. He played a key role in setting up the Microelectronics Centre at IIT for carrying out experimental research in silicon devices and ICs. He has conducted many students' projects and PhD programmes in the areas of microelectronics and SAW devices and led research teams to undertake sponsored R&D programmes in bipolar device modelling and

process simulation. His current research activities include integrated optics, power ICs, special semiconductor films, microsensors and MEMs. He is working in close collaboration with DRDO, ISRO, industries like BEL, Bangalore. He has published about eighty research papers. He has served as a member of National Microelectronics Council Technology Working Group, CSIR Manpower Assessment Board, Board of Examiners of several universities and Project Review Committees of DOE and ISRO.